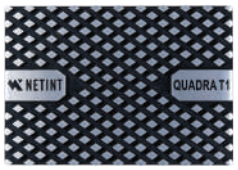
Quadra T1/T1A/T2A Video Processing Unit Datasheet.

- Quadra VPUs are built on the newest NETINT Codensity™ G5 ASIC, optimized for enterprise-class video transcoding at up to 8Kp60.
- Realtime and ultra-low latency video platforms and services can utilize Quadra VPUs in their x86 and Arm-based servers to reduce operational costs by as much as 40X, and carbon emissions 80X compared to software-based video transcoders, while maintaining broadcast video quality.
- The Quadra VPUs feature scalable levels of performance in PCIe 2.5" U.2 and AIC form factors and are a flexible and simple solution for video encoding and processing in the data center.



Quadra T1

Quadra T1A

Quadra T2A

Features and Performance

Video Encoding Standards/Formats

AVC/H.264 Baseline, Main, High, High 10
HEVC/H.265 Main, Main 10
AV1 Main
JPEG
YUV 420 8 bit/10 bit Encoding

T1 Throughput: Up to 16x 1080p60, 4x 4Kp60, 1x 8Kp60
T1A Throughput: Up to 16x 1080p60, 4x 4Kp60, 1x 8Kp60
T2A Throughput: Up to 32x 1080p60, 8x 4Kp60, 2x 8Kp60

HDR10/10+, HLG
HRD, VBR, FIXQP, CBR, CRF, ROI
SEI/Meta Data Insertion
Closed Captions
AI Assisted Encoding
Look Ahead

Video Decoding Standards/Formats

AVC/H.264 Baseline, Main, High, High 10
HEVC/H.265 Main, Main 10
VP9 Profile 0, Profile 2
JPEG
YUV 420 8 bit/10 bit Decoding

T1 Throughput: Up to 24x 1080p60, 6x 4Kp60, 1x 8Kp90
T1A Throughput: Up to 24x 1080p60, 6x 4Kp60, 1x 8Kp90
T2A Throughput: Up to 48x 1080p60, 12x 4Kp60, 2x 8Kp90

HDR10/10+, HLG
SEI/Meta Data Extraction
Closed Captions
Error Concealment

Video 2D Processing Engines

Cropping and Padding
Scaling
Video Overlay
YUV and RGB Conversion

Software Integration

Windows, MacOS, Linux and Android OS Support
Virtual machine and container virtualization support
Single Root I/O Virtualization [SRIOV]
libxcoder API for encoding, decoding, 2D and AI support
Libavcodec, a library of codecs, for video and audio
FFmpeg Versions 3.4.2, 4.1.3, 4.2.1, 4.3, 4.3.1, 4.4 and 5.0
GStreamer integration

System Requirements

-Intel i5 CPU or equivalent
-8GB DDR4 RAM
-For best performance PCIe Gen4 x8 or x16 slot

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Quadra T1/T1A/T2A VPU Datasheet - V1.0

Preliminary Data Subject to Change.

Quadra T1/T1A/T2A Video Processing Unit Datasheet.

Technical Specifications

Physical Dimensions	Quadra T1	Quadra T1A	Quadra T2A
Form Factor	U.2 2.5-inch	HHHL AIC Form Factor	HHHL AIC Form Factor
Dimensions	100x70x15mm	168x80x19mm	168x80x19mm
Weight	190 Grams	297 Grams	307 Grams
Power	17W Typical Under Full Load	20W Typical Under Full Load	40W Typical Under Full Load
Compliance	NVM Express 1.3 PCI Express 4.0 PCI Express Card Electro-Mechanical Spec. V4.0 Enterprise SSD Form Factor V1.a	NVM Express 1.3 PCI Express 4.0 PCI Express Card Electro-Mechanical Spec. V4.0	NVM Express 1.3 PCI Express 4.0 PCI Express Card Electro-Mechanical Spec. V4.0
Temperature	Operation Ambient Temperature: 0 to 50° C Non-Operation Ambient Temperature: -55 to 95° C Temperature monitoring (In-band and out of band) Thermal Throttling Activation: 70° C composite temperature Thermal Shutdown: 80° C composite temperature		

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Quadra T1/T1A/T2A Video Processing Unit Datasheet.

Artificial Intelligence Deep Neural Network Inference Engines

T1: INT8 Trillion Operations Per Second (TOPs): 18 TOPS
T1A: INT8 Trillion Operations Per Second (TOPs): 18 TOPS
T2A: INT8 Trillion Operations Per Second (TOPs): 36 TOPS

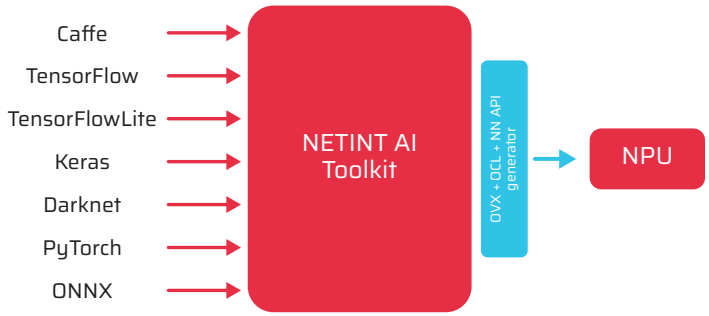
AI deep learning models imported to Quadra VPUs with the NETINT AI Toolkit then processed (Import, quantization, validation and optimization), exported, and executed on Quadra Neural Processing Units (NPUs).

All major deep learning frameworks supported for model training

Caffe
TensorFlow
TensorFlow Lite
Keras
Darknet
PyTorch
ONNX

NETINT AI Tool Chain

All major deep learning frameworks supported for model training.



Applications for AI models can include:

ROI-Encoding
Scene Detection
Background Removal
Video Enhancement
Facial Recognition
Object Detection

Quadra NPU pre-trained AI model deployment flow

Step 1 Import a trained model → **Step 2** Quantize an imported model → **Step 3** Export for hardware deployment

Supported Frameworks:

- ONNX
- TFLite
- PyTorch
- Darknet
- TensorFlow
- Keras

Features:

- 8 bit / 16 bit Quantization
- Hybrid Quantization
- Accuracy Validation
- Graph Optimization
- Pre-Processing integration

Features:

- Hardware-aware Optimization
- Execution Graph Generator
- Performance Profiling
- Python/C Inference API

Model Performance on Quadra

- AI Capability per G5 ASIC:18 TOPs
- Datatype for evaluation: INT8
- Test hardware: T1A
- Test firmware version: 3.1

Specification	Yolov5s	Yolov5s	Yolov4-tiny	ResNet 50	MobileNetv2	FSRCNNx3	DeepLabv3	BiSeNetV1	HrNet
Input Size	640x640	320x320	416x416	224x224	224x224	360x640	257x257	512x512	256x192
Data type	INT8	INT8	INT8	INT8	INT8	INT8	INT8	INT8	INT8
Batch Size	1	1	1	1	1	1	1	1	1
Performance (FPS@1GHz)	78	231	276	228	1234	36	452	51	72

- **Performance is based on original model without pruning / sparsity / modification.**

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Quadra T1/T1A/T2A VPU Datasheet - V1.0

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Quadra T1/T1A/T2A Video Processing Unit Datasheet.

PCI-Express Information

- The T2A and T1A AIC both comply with the PCI-Express CEM 4.0 standard.
- The T1A AIC is a 4 lane PCI-Express Gen 4 interface.
- The T2A AIC is a 2x4 lane Gen 4 interface, and requires bifurcation in order to recognize both the Quadra devices in the AIC card.

PCI-Express ID Information

Device ID = 0401h
Vendor ID= 1D82h

Certifications and Declarations

Certification	Quadra T1/T1A/T2A
CE Compliant	European Economic Area (EEA): Compliance with the essential requirements of Multimedia Equipment (MME) EN 55032:2015+A11:2020 EN 55035:2017+A11:2020
FCC Compliant	USA: Compliance with following standard: 47 CFR FCC part 15 subpart B, 10-1-2021 ANSI C63.4:2014 Class B
UL Recognized	Certified Underwriters Laboratories, Inc. Bi-National Component Recognition; IEC 62368-1:2014 (Audio/video, information and communication technology equipment - Part 1: Safety requirements) EN 62368-1:2014 + A11:2017, AS/NZS 62368.1:2018, J62368-1 (2020). CSA/UL 62368-1: 2014
RoHS Compliant	Restriction of Hazardous Substance Directive. Directive 2011/65/EU Meets requirements of European Union (EU) ROHS Compliance Directives

Quadra T1/T1A/T2A Video Processing Unit Datasheet.

Appendix

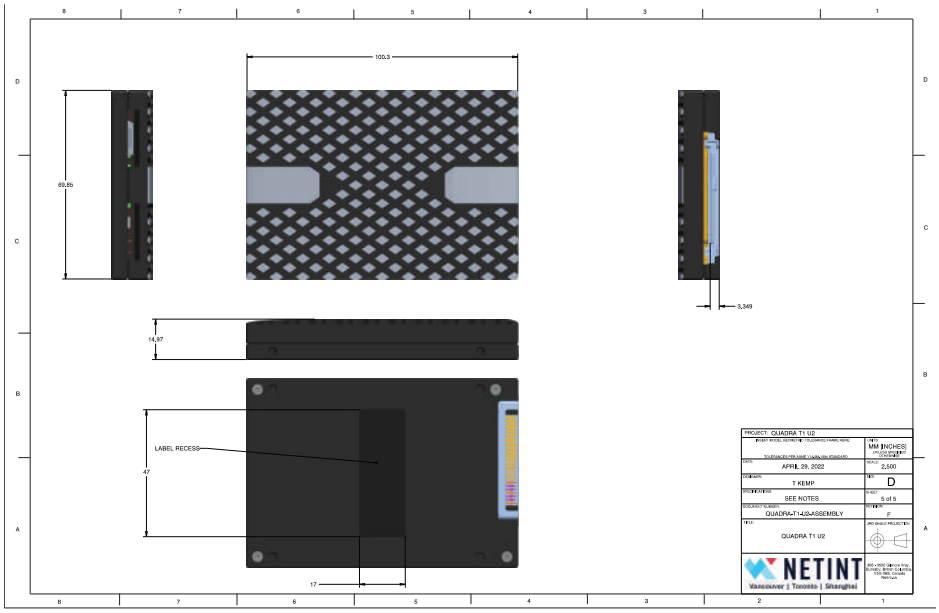
Electrical Characteristics

Input Supply Rails

Electrical Characteristics	Quadra T1		Quadra T1A		Quadra T2A	
Supply Rail	**12V Host**	**3.3V Aux**	**12V Host**	**3.3V Aux**	**12V Host**	**3.3V Aux**
Tolerance	±8%	±9%	±8%	±9%	±8%	±9%
Max Startup Current (first 2s operating)	2.1A	-	2.75A	-	5.5A	-
Max Average Current	2.1A	1mA active/inactive	2.75A	1mA active/inactive	5.5A	1mA active/inactive
Rising Slew Rate	250V/s - 420kV/s	250V/s - 420kV/s	250V/s - 420kV/s	250V/s - 420kV/s	250V/s - 420kV/s	250V/s - 420kV/s
Falling Slew Rate	2.4 V/s - 250kV/s	0.66V/s - 33kV/s	2.4 V/s - 250kV/s	0.66V/s - 33kV/s	2.4 V/s - 250kV/s	0.66V/s - 33kV/s
Shutdown Undershoot	0V (No undershoot allowed)	0V (No undershoot allowed)	0V (No undershoot allowed)	0V (No undershoot allowed)	0V (No undershoot allowed)	0V (No undershoot allowed)
Noise 10Hz - 100kHz	1000mV	300mV	1000mV	300mV	1000mV	300mV
Noise 100kHz - 20MHz	50mV	50mV	50mV	50mV	50mV	50mV

Mechanical Information

Physical package information for Quadra T1 form factor. All dimensions are in millimeters.



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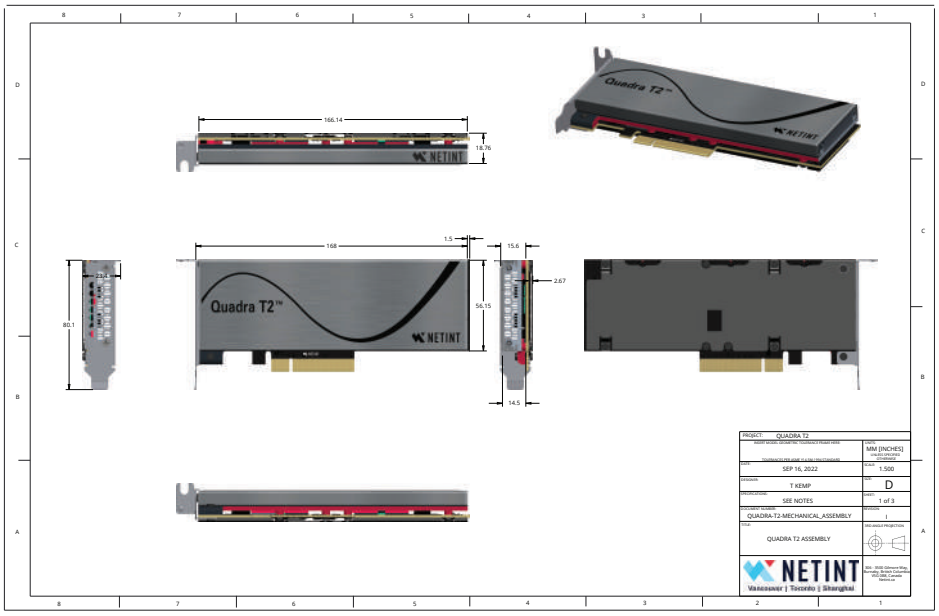
Quadra T1/T1A/T2A Video Processing Unit Datasheet.

Appendix

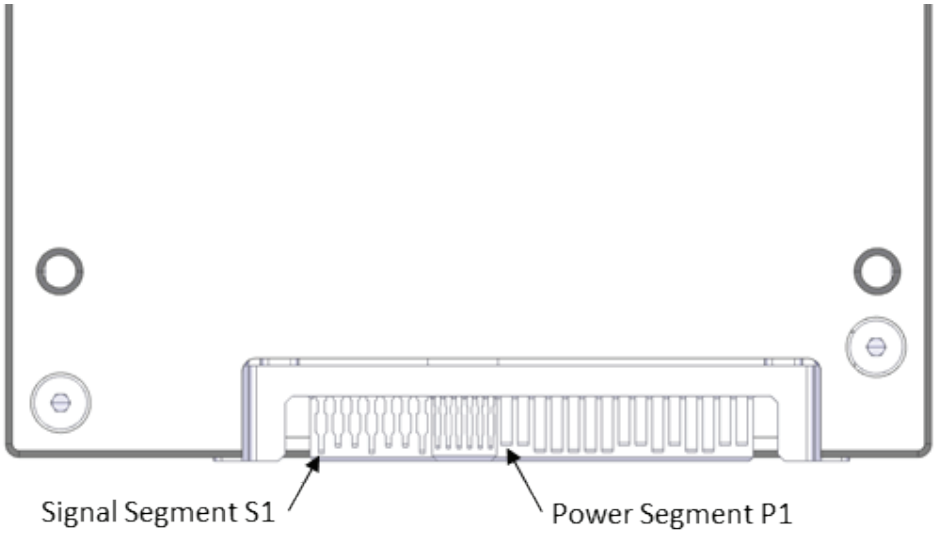
Physical package information for Quadra T1A/T2A form factor. All dimensions are in millimeters.



Pin and Signal Descriptions

U.2 2.5-inch Form Factor Pin Locations

Layout of 2.5-inch Form Factor Signal and Power Segment Pins (U.2 SFF-8639).



Note: 2.5-inch connector supports built in latching capability.

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Quadra T1/T1A/T2A Video Processing Unit Datasheet.

Appendix

Pin and Signal Descriptions

Pin Definition for Quadra T1, U.2 Form Factor

Pin	Name	Definition	Pin	Name	Definition
S1	GND	Ground	E7	REFCLK0+	PCIe clock port 0 p
S2	SOT+	Open (SATA/SAS)	E8	REFCLK0-	PCIe clock port 0 n
S3	SOT-	Open (SATA/SAS)	E9	GND	Ground
S4	GND	Ground	E10	PETp0	PCIe TX Lane 0 p
S5	SOR-	Open (SATA/SAS)	E11	PETn0	PCIe TX Lane 0 n
S6	SOR+	Open (SATA/SAS)	E12	GND	Ground
S7	GND	Ground	E13	PERn0	PCIe RX Lane 0 n
E1	REFCLK1+	Open	E14	PERp0	PCIe RX Lane 0 p
E2	REFCLK1-	Open	E15	GND	Ground
E3	3.3Vaux	3.3V auxiliary power	E16	RSVD	Open
E4	PERST1#	Pull Low	S8	GND	Ground
E5	PERST0#	PCIe Fundamental Reset	S9	S1T+	Open (SATA/SAS)
E6	RSVD	Open	S10	S1T-	Open (SATA/SAS)
P1	RSVD(Wake#)	Open	S11	GND	Ground
P2	sPCIeRst	Open	S12	S1R-	Open (SATA/SAS)
P3	RSVD(ClkReq#)	Open	S13	S1R+	Open (SATA/SAS)
P4	IfDet#	Ground (Enterprise PCIe)	S14	GND	Ground
P5	GND	Ground	S15	RSVD	Open
P6	GND	Ground	S16	GND	Ground
P7	5V	Open (SATA/SAS)	S17	PETp1	PCIe TX Lane 1 p
P8	5V	Open (SATA/SAS)	S18	PETn1	PCIe TX Lane 1 n
P9	5V	Open (SATA/SAS)	S19	GND	Ground
P10	PRSNT#	Open (Enterprise PCIe)	S20	PERn1	PCIe RX Lane 1 n
P11	Activity	Activity	S21	PERp1	PCIe RX Lane 1 p
P12	Hot-Plug	Ground	S22	GND	Ground
P13	12V_pre	12V power	S23	PETp2	PCIe TX Lane 2 p
P14	12V	12V power	S24	PETn2	PCIe TX Lane 2 n
P15	12V	12V power	S25	GND	Ground
			S26	PERn2	PCIe Rx Lane 2 n
			S27	PERp2	PCIe RX Lane 2 p
			S28	GND	Ground
			E17	PETp3	PCIe TX Lane 3 p
			E18	PETn3	PCIe TX Lane 3 n
			E19	GND	Ground
			E20	PERn3	PCIe RX Lane 3 n
			E21	PERp3	PCIe RX Lane 3 p
			E22	GND	Ground
			E23	SMCLK	SMBus clock
			E24	SMDAT	SMBus data
			E25	DualPortEn#	Open